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METHOD OF FABRICATING A POLYSILICON CAPACITOR UTILIZING FET AND BIPOLAR BASE POLYSILICON LAYERS

ABSTRACT OF THE DISCLOSURE

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A method of forming a poly-poly capacitor, a MOS transistor, and a bipolar transistor simultaneously on a substrate comprising the steps of depositing and patterning a first layer of polysilicon on the substrate to form a first plate electrode of said capacitor and on an electrode of the MOS transistor, and depositing and patterning a second layer of polysilicon on the substrate to form a second plate electrode of said capacitor and an electrode of the bipolar transistor.